

# Fourth International Workshop on FPGAs for Software Programmers (FSP 2017)

September 7, 2017, Ghent, Belgium

co-located with

International Conference on Field Programmable Logic and Applications (FPL)

## Call for Papers

The aim of this one-day workshop is to make FPGA and reconfigurable technology accessible to software programmers. Despite their frequently proven power and performance benefits, designing for FPGAs is mostly an engineering discipline carried out by highly trained specialists. With recent progress in high-level synthesis, a first important step towards bringing FPGA technology to potentially millions of software developers was taken. However, to make this happen, there are still important issues to be solved that are in the focus of this workshop.

The FSP Workshop aims at bringing researchers and experts from both academia and industry together to discuss and exchange the latest research advances and future trends. This includes high-level compilation and languages, design automation tools that raise the abstraction level when designing for (heterogeneous) FPGAs and reconfigurable systems and standardized target platforms. This will in particular put focus on the requirements of software developers and application engineers. In addition, a distinctive feature of the workshop will be its cross section through all design levels, ranging from programming down to custom hardware. Thus, the workshop is targeting all those who are interested in understanding the big picture and the potential of domain-specific computing and software-driven FPGA development. In addition, the FSP Workshop shall facilitate collaboration of the different domains.

Topics of the FSP Workshop include, but are not limited to:

- High-level synthesis and domain-specific languages (DSLs) for FPGAs and heterogeneous systems
- Mapping approaches and tools for heterogeneous FPGAs
- Support of hard IP blocks such as embedded processors and memory interfaces
- Development environments for software engineers (automated tool flows, design frameworks and tools, tool interaction)
- FPGA virtualization (design for portability, hardware abstraction etc.)
- Design automation for multi-FPGA and heterogeneous systems
- Methods for leveraging (partial) dynamic reconfiguration to increase performance, flexibility, reliability, or programmability
- Operating system services for FPGA resource management, reliability, security
- Target hardware design platforms (infrastructure, drivers, portable systems)
- Overlays (CGRAs, vector processors, ASIP-/GPU-like intermediate fabrics)
- Applications (embedded computing, signal processing, big data, bio informatics, database acceleration etc.) using OpenCL, OpenSPL, Vivado-HLS etc.
- Directions for collaborations (research proposals, networking, Horizon 2020)

### Paper submission

Perspective authors are invited to submit original contributions (up to eight pages) or extended abstracts describing work-in-progress or position papers (not exceeding two pages).

Details about the submission process are available on the workshop web page.

### Publications

The proceedings of this workshop containing all accepted papers are planned to be published by VDE-Verlag (Germany) and are planned to be indexed by IEEE Xplore. Every accepted paper must have at least one author registered to the workshop by the time the camera-ready paper is due.

## Organization

### General Co-Chairs

Andreas Koch  
*Technische Universität Darmstadt, Germany*  
Markus Weinhardt  
*Osnabrück Univ. of Appl. Sciences, Germany*

### Proceedings Chair

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*Mannheim Univ. of Appl. Sciences, Germany*  
Peter Yiannacouras  
*Altera Corp., Canada*  
Daniel Ziener  
*University of Erlangen-Nürnberg, Germany*

### Important dates

Submission deadline: June 25, 2017  
Notification of acceptance: July 30, 2017  
Camera-ready final version: August 8, 2017

### For more information visit

<http://www.fsp-workshop.org>