

Fourth International Workshop on
FPGAs for Software Programmers (FSP 2017)

September 7, 2017, Ghent, Belgium

co-located with

International Conference on Field Programmable Logic and Applications (FPL)

Program

- 09:00 – 09:05 Workshop Opening
- 09:05 – 10:00 **KEYNOTE 1: "FPGA-supported domain-specific embedded computing"**
Dirk van den Heuvel, TOPIC Products
- 10:00 – 10:30 **"Spatial Memory Trace Prediction"**
Nadeen Yassir Gebara, Paolo lenne, Kermin Fleming
- 10:30 – 11:00 Coffee Break
- 11:00 – 11:30 **"A Case for Better Integration of Host and Target Compilation When Using OpenCL for FPGAs"**
Taylor Lloyd, Artem Chikin, Erick Ochoa, Karim Ali, José Nelson Amaral
- 11:30 – 12:00 **"PCIeHLS: an OpenCL HLS framework"**
Malte Vesper, Dirk Koch, Khoa Pham
- 12:00 – 12:30 **"SOCAO: Source-to-Source OpenCL Compiler for Intel-Altera FPGAs"**
Johanna Rohde, Marcos Martinez-Peiró, Rafael Gadea-Gironés
- 12:30 – 14:00 Lunch
- 14:00 – 14:55 **KEYNOTE 2: "FPGA-based Acceleration: we need source to source compilers!"**
João M.P. Cardoso, University of Porto/FEUP/INESC-TEC
- 14:55 – 15:10 **"C++ support for better hardware/software co-design in C# with SME"**,
Kenneth Skovhede, Brian Vinter (Short Paper)
- 15:10 – 15:25 **"On the HLS Design of Bit-Level Operations and Custom Data Types"**,
Jose Raul Garcia Ordaz, Dirk Koch (Short Paper)
- 15:25 – 15:50 Coffee Break
- 15:50 – 16:20 **"A Highly Efficient and Comprehensive Image Processing Library for C++-based High-Level Synthesis"**
M. Akif Özkan, Oliver Reiche, Frank Hannig, Jürgen Teich
- 16:20 – 16:50 **"Accelerating Linux Bash Commands on FPGAs Using Partial Reconfiguration"**
Edson Horta, Xinzi Shen, Khoa Pham, Dirk Koch
- 16:50 – 17:20 **"Acceleration of Solving Quadratic Assignment Problems on Programmable SoC using High Level Synthesis"**
Kenji Kanazawa
- 17:20 – 17:35 **"Using GCC Analysis Techniques to Enable Parallel Memory Accesses in HLS"**
Johanna Rohde, Christian Hochberger (Short Paper)
- 17:35 – 17:40 Workshop Closing

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