Sixth International Workshop on

FPGAs for Software Programmers (FSP 2019)

September 12, 2019, Barcelona, Spain

co-located with

International Conference on Field Programmable Logic and Applications (FPL)

Program

09:00 – 09:05 Workshop Opening

09:05 – 10:05 **KEYNOTE 1: "Addressing High-level Synthesis Challenges for Heterogenous Computing at the Edge"**
Juan Eusse, Silexica, Germany

10:05 – 11:50 **Session 1: HLS Acceleration and Optimization**

10:05 – 10:30 **"Accelerating Human Activity Recognition Systems on FPGAs through a DSL approach"**
Daniel Fernandes and João Cardoso

10:30 – 11:00 Coffee Break

11:00 – 11:25 **"Accelerating Design Convergence of Automata Processing Designs with a Tiled Hierarchy"**
Tommy Tracy II, Jack Wadden, Ted Xie, Kevin Skadron and Mircea Stan

11:25 – 11:50 **"Impact of Off-Chip Memories on HLS-Generated Circuits"**
Abhi *D. R., Ron Sass and Andrew Schmidt*

11:50 – 13:05 **Session 2: Heterogeneous Systems and Runtime Support**

11:50 – 12:15 **"LibGalapagos: A Software Environment for Prototyping and Creating Heterogeneous FPGA and CPU Applications"**
Naif Tarafdar and Paul Chow

12:15 – 12:40 **"Run-time Performance Monitoring of Heterogenous Hw/Sw Platforms Using PAPI"**
Tiziana Fanni, Daniel Madroñal, Claudio Rubattu, Carlo Sau, Francesca Palumbo, Eduardo Juárez, Maxime Pelcat, César Sanz and Luigi Raffo

12:40 – 13:05 **"ZUCL 2.0: Virtualised Memory and Communication for ZYNQ UltraScale+ FPGAs"**
Khoa Pham, Kyriakos Paraskevas, Anuj Vaishnav, Andrew Attwood, Malte Vesper and Dirk Koch

13:05 – 14:00 Lunch Break

14:00 – 15:00 **KEYNOTE 2: "Architecture Virtualization as Prerequisite for Large-Scale FPGA Adoption In Software Communities"**
Christophe Bobda, University of Florida, USA

15:00 – 15:30 **INVITED TALK: "fpgaConvNet and f-CNN^{x}: Towards addressing the challenges in ML application deployment"**
Christos-Savvas Bouganis, Imperial College, London, UK

15:30 – 16:00 Coffee Break

16:00 – 16:45 **TUTORIAL: "OpenCL design flows for Intel and Xilinx FPGAs - using common design patterns and dealing with vendor-specific differences"**
Tobias Kenter, Paderborn University, Germany

16:45 – 17:15 **INVITED TALK: "Care of magical creatures - How to tame, train and feed your Alveo or Stratix FPGA card"**
Luciano Lavagno, Politecnico di Torino, Italy

17:15 – 17:30 Workshop Closing

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